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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/682,558 | 10/09/2003 | Arnaldo R. Cruz | SC13055TH | 9462 |

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| EXAMINER | |
|---|---|
| PATEL, NIMESH G | |
| **ART UNIT** | **PAPER NUMBER** |
| 2112 | |

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/682,558 | CRUZ ET AL. | |
| | Examiner | Art Unit | |
| | Nimesh G. Patel | 2112 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) *29-37* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## *Conclusion*

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election with traverse of Invention I in the reply filed on January 12, 2006 is acknowledged. The traversal is on the ground(s) that the separate utility of Invention II is functions that can be performed by Invention I. This is not found persuasive because the combination(Invention I) as claimed does not require the particulars of the subcombination(Invention II) as claimed. The subcombination has separate utility such as interrupt processing and steering in as USB shared configurable resource.

The requirement is still deemed proper and is therefore made FINAL.

2. Claims 29-37 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected Invention II, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on January 12, 2006.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Jeansonne et al.(US20040205280).

5. Regarding claim 1, Jeansonne discloses a data processing system, comprising: a first bus master; a second bus master(Paragraph 17, processors); and a shared reconfigurable resource(Figure 2, 40) accessible by the first bus master and the second bus master(Figure 2, 42) wherein the shared reconfigurable resource establishes a communication path between at least one of the first and second bus masters and circuitry for performing a first peripheral function selected from a plurality of peripheral functions(Paragraph 22, Figure 2).

6. Regarding claim 2, Jeansonne discloses a data processing system, wherein the shared reconfigurable resource comprises reconfigurable channel circuitry(Figure 2, 65) which comprises at least a portion of the circuitry for performing the first peripheral function(Figure 2, 62).

7. Regarding claim 3, Jeansonne discloses a data processing system, wherein the shared reconfigurable resource comprises reconfigurable channel storage accessible by the reconfigurable channel circuitry for use in performing the first peripheral function(Paragraph 24).

8. Regarding claim 4, Jeansonne discloses a data processing system, wherein the reconfigurable channel circuitry is configurable to perform a second peripheral function selected from the plurality of peripheral functions(Figure 2, 64).

9. Regarding claim 5, Jeansonne discloses a data processing system, wherein the shared reconfigurable resource establishes a second communication path between at least one of the first and second bus masters and circuitry for performing the second peripheral function(Figure 2, 64), and wherein the reconfigurable channel circuitry comprises at least a portion of the circuitry for performing the second peripheral function(Figure 2, 40).

10. Regarding claim 6, Jeansonne discloses a data processing system, wherein the circuitry for performing the second peripheral function comprises at least one of a serial peripheral interface (SPI), a universal asynchronous receiver/transmitter (UART), a universal serial bus

(USB), an input capture, an output compare, a general purpose input/output, a timer, and a synchronous serial interface (SSI)(Paragraph 23).

11. Regarding claim 7, Jeansonne discloses a data processing system, wherein the data processing system further comprises first peripheral function circuitry coupled to the shared reconfigurable resource, wherein the first peripheral function circuitry comprises at least a first portion of the circuitry for performing the first peripheral function(Figure 2, 62).

12. Regarding claim 8, Jeansonne discloses a data processing system, wherein the shared reconfigurable resource comprises at least a second portion of the circuitry for performing the first peripheral function(Figure 2, 40).

13. Regarding claim 9, Jeansonne discloses a data processing system, wherein the shared reconfigurable resource establishes a second communication path between at least one of the first and second bus masters and circuitry for performing a second peripheral function selected from the plurality of peripheral functions(Figure 2, 64).

14. Regarding claim 10, Jeansonne discloses a data processing system, wherein the data processing system further comprises second peripheral function circuitry(Figure 2, 64) coupled to the shared reconfigurable resource, wherein the second peripheral function circuitry comprises at least a first portion of the circuitry for performing the second peripheral function and the shared reconfigurable resource comprises at least a second portion of the circuitry for performing the second peripheral function(Figure 2, 40).

15. Regarding claim 11, Jeansonne discloses a data processing system, wherein the circuitry for performing the second peripheral function comprises at least one of a serial peripheral interface (SPI), a universal asynchronous receiver/transmitter (UART), a universal serial bus (USB), an input capture, an output compare, a general purpose input/output, a timer, and a synchronous serial interface (SSI)(Paragraph 23).

16. Regarding claim 12, Jeansonne discloses a data processing system, wherein the circuitry for performing the first peripheral function comprises at least one of a serial peripheral interface (SPI), a universal asynchronous receiver/transmitter (UART), a universal serial bus (USB), an input capture, an output compare, a general purpose input/output, a timer, and a synchronous serial interface (SSI)(Paragraph 23).

17. Claims 13-21 are directed to the method of data processing system claims 1-13 and claims 22-28 are directed to the shared reconfigurable resource of data processing system claims 1-13. Jeansonne discloses the data processing system as set forth in claims 1-13. Therefore, Jeansonne also discloses the method as set forth in claims 13-21 and a shared reconfigurable resources as set forth in claims 22-28.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nimesh G. Patel whose telephone number is 571-272-3640. The examiner can normally be reached on M-F, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nimesh G Patel
Examiner
Art Unit 2112

NP
April 3, 2006

Glenn A. Auve
Primary Patent Examiner
Technology Center 2100